ATS2815 Datasheet

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Revision History

Date	Revision	Description
2016-6-23	1.0	First Release

1 Introduction

Features

- 156MHz 32bit RISC processor Core
- Internal ROM
- Internal RAM for data and program
- Bluetooth 4.2 dual mode support: simultaneous LE and BR/EDR
- Compatible with Bluetooth V4.1/4.0/2.1+EDR
- Supports AFH to dynamically detect channel quality to improve Bluetooth transmission quality
- Bluetooth Piconet and Scatternet support
- Maximum Bluetooth TX power: >4dBm
- Bluetooth RX sensitivity: <-88dBm
- Built-in high performance DAC & ADC
- Supports single-ended Analog microphone
- Integrated PMU supports multiple low energy states
- Linear regulators outputs
- Support low power mode (sniff/sniff sub-rating)
- Standby current 35uA (typical).
- Support SD/MMC/eMMC card interface
- Serial Interfaces: USB1.1FS, UART, TWI
- QFN-40, 5mm*5mm

Actions® ATS2815™ QFN40

Bluetooth Audio Solution

Wireless Audio Applications
MMC/SD Card Audio Playback

Bluetooth V4.2

Applications

- Stereo speakers and speakerphones
- Bluetooth car audio unit
- Other Bluetooth applications

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1.1 Overview

The ATS2815 is a highly integrated single-chip Bluetooth audio device. It also can act as traditional card speakers and card-reader for data transmission.

The ATS2815 integrates the high-performance transceiver, rich features baseband processor and Bluetooth audio profile. It meets V4.2 and complies with V4.1/4.0/2.1+EDR, it is also completely backward compatible with Bluetooth V1.1/1.2/2.0 specification. It supports dual mode (BR/EDR), and the links in BR/EDR and LE can be active simultaneously.

ATS2815 integrates high quality and low latency SBC decoder and CVSD codec. It also supports PLC technique and AEC in voice call providing a high audio quality.

The ATS2815 integrates a complete set of power management circuits, flexible memory configuration, and rich interfaces, such as SD/MMC card/USB/UART/TWI and so on. The architecture is fully programmable with any application. It also has the minimum package and the most compact BOM.

1.2 Application Diagram

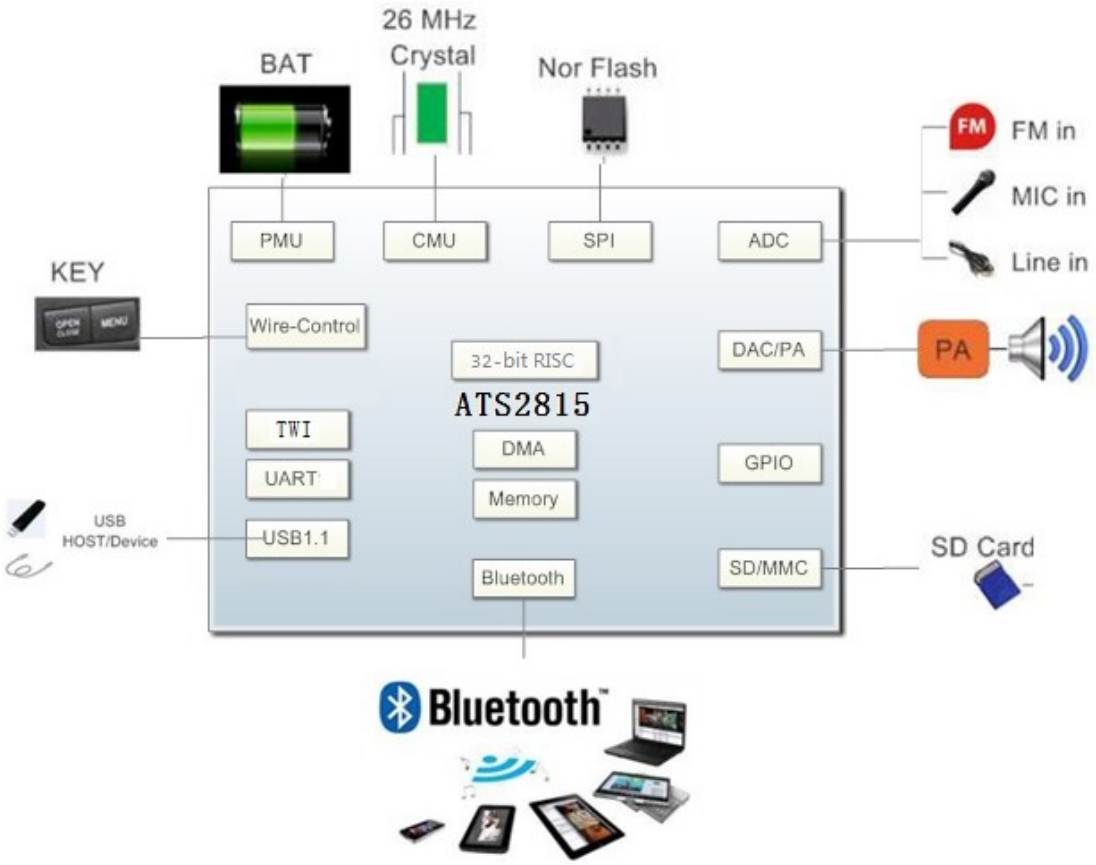


Figure 1-1 ATS2815 Application Diagram

1.3 Detail Features

System

- 156MHz 32bit RISC processor Core
- Internal RAM for data and program storage
- 4-channel DMA, including DMA0, DMA1, DMA2 and DMA3, support for transmission in burst 8 mode
- Fully configurable PEQ, up to 14 segments
- Support for echo cancellation and noise reduction
- Support for packet loss concealment

Bluetooth

- Support Bluetooth v4.2 Low Energy (BLE)
- Compatible with Bluetooth V4.1/4.0/2.1+EDR
- Bluetooth 4.2 dual mode support: simultaneous LE and BR/EDR
- Support all packet types in basic rate and enhanced data rate
- Support SCO/eSCO link
- Support secure simple pairing
- Support low power mode (sniff/sniff sub-rating)
- Bluetooth Piconet and Scatternet support
- Maximum Bluetooth TX power: >4dBm
- Bluetooth RX sensitivity: <-88dBm

Audio

- Built-in stereo 16-bit input sigma-delta DACs, SNR>92dB, SNR (A-Weighting)>95dB, THD+N < -81dB
- Built-in mono 16-bit input sigma-delta ADC, SNR>85dB, SNR(A-Weighting)>88dB, THD+N < -72dB
- DAC supports sample rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48 kHz
- ADC supports sample rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48 kHz

Package

- QFN-40, 5mm*5mm

Power Management

- Support Li-Ion battery power supply with battery insert wake up.
- Support power on button & reset button.
- Linear regulator output VCC.
- Linear regulators outputs AVCC, VDD
- Standby current 35uA (typical).
- Low resolution 7-bit A/D converters for system monitor and wire-control.

Physical Interfaces

- 1*SD/MMC/eMMC card interface
- USB1.1FS host or device, support 2 IN endpoint and 1 OUT endpoint except endpoint0
- 1*UART support master or slave mode with RTS/CTS hardware flow control
- 1*TWI supports slave function
- Support 15 GPIO interfaces
- 2*SIRQ supported
- 1*PWM output integrated

1.4 Pin Assignment

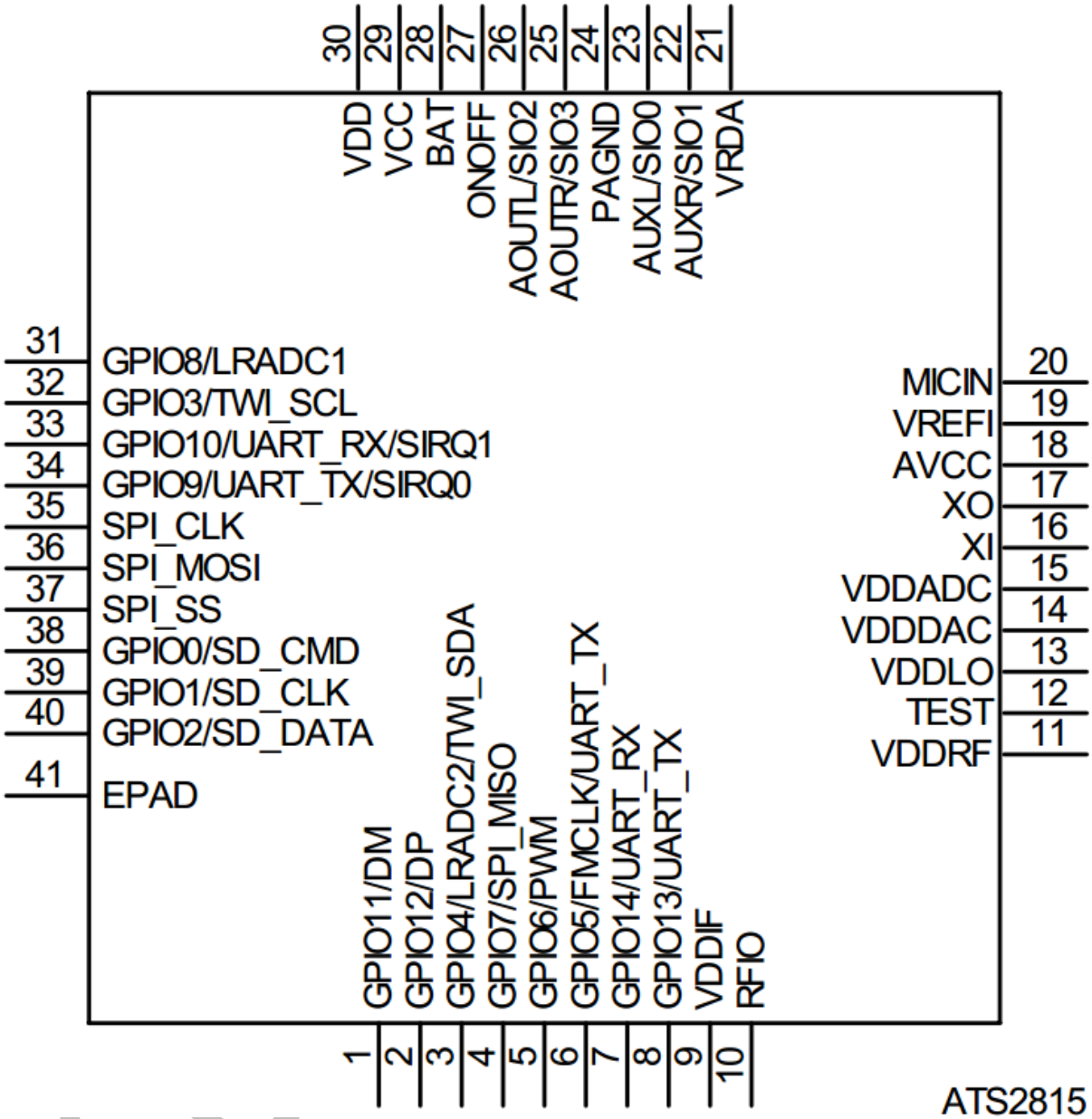


Figure 1-2 ATS2815 Pin Assignment

1.5 Pin Descriptions

Table 1-1 ATS2815 Pin Description

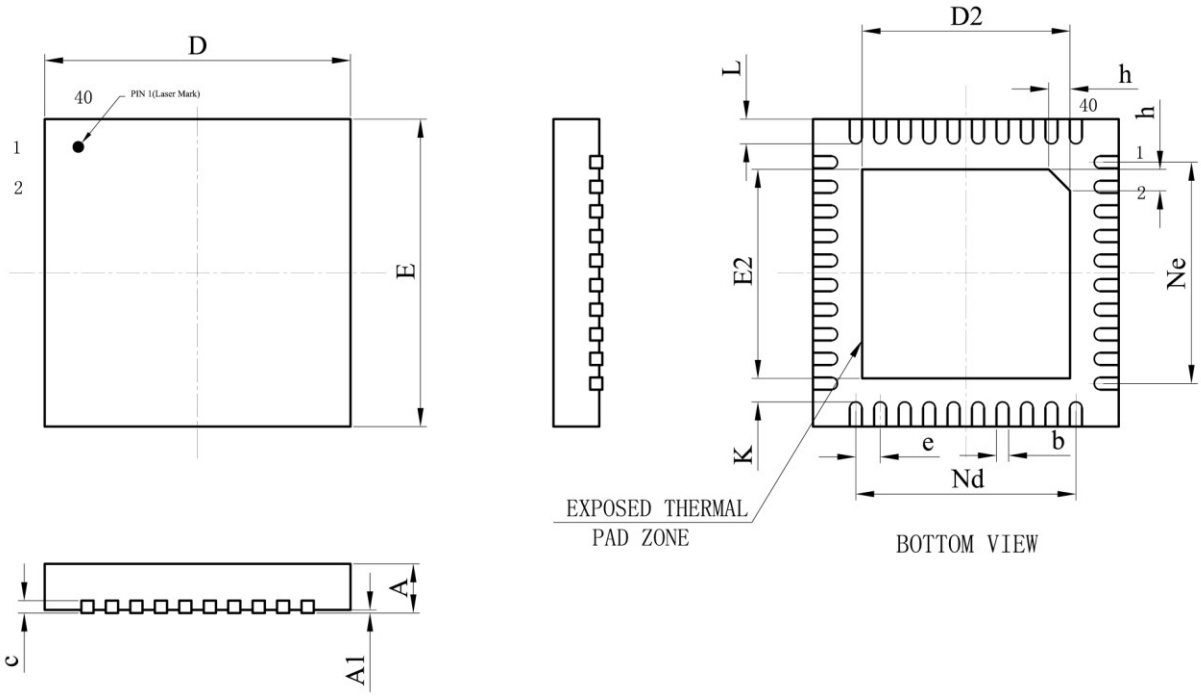
Pin No.	Pin Name	Pin Type	Function Mux	Pad drive level	GPIO Initial State	Description
1	GPIO11	I/O	DM/UART_CTS	2/4/6/8/10/12/14/16mA	Z	Bit11 of GPIO 1.USB data minus 2.UART_CTS
2	GPIO12	I/O	DP/UART_RTS	2/4/6/8/10/12/14/16mA	Z	Bit12 of GPIO 1.USB data plus 2.UART_RTS

3	GPIO4	A/I/O	TWI_SDA/UART_RX/PWM/LRADC2	2/4/6/8/10/12/14/16mA	Z	Bit4 of GPIO 1.TWI_SDA 2.UART_RX 3.PWM 4.LRADC2: Low resolution A/D input 2
4	GPIO7	I/O	UART_RTS/PWM/SPI_MISO	2/4/6/8/10/12/14/16mA	Z	Bit7 of GPIO 1.UART_RTS 2.PWM 3.SPI_MISO
5	GPIO6	A/I/O	UART_CTS/PWM/SIRQ1	2/4/6/8/10/12/14/16mA	Z	Bit6 of GPIO 1.UART_CTS 2.PWM 3.SIRQ1
6	GPIO5	I/O	FMCLKOUT/UART_TX/SIRQ0/PWM	2/4/6/8/10/12/14/16mA	Z	Bit5 of GPIO 1.FMCLKOUT 2.UART_TX 3.SIRQ0 4.PWM
7	GPIO14	I/O	UART_RX	2/4/6/8/10/12/14/16mA	Z	Bit14 of GPIO 1.UART_RX
8	GPIO13	I/O	UART_TX	2/4/6/8/10/12/14/16mA	Z	Bit13 of GPIO 1.UART_TX
9	VDDIF	PWRI				IF Power
10	RFIO	I/O				Bluetooth transmitter output/receiver input
11	VDDRF	PWRI				RF Power
12	TEST	I/O				Test pin
13	VDDLO	PWRI				LO Power
14	VDDDAC	PWRI				DAC Power
15	VDDADC	PWRO				ADC Power
16	XI	AI	XI			High frequency crystal OSC input
17	XO	AO	XO			High frequency crystal OSC output
18	AVCC	PWRO				Power supply of Analog
19	VREFI	AO				Voltage reference
20	MICIN	A/I/O				Microphone input
21	VRDA	AO				Audio reference voltage
22	AUXR	A/I/O	AUXR/SIO1	2/4/6/8/10/12/14/16mA		Right channel of AUX input

23	AUXL	A/I/O	AUXL/SIO0	2/4/6/8/10/12/14/16 mA		Left channel of AUX input
24	PAGND	GND				Power Amplify GND
25	AOUTR	A/I/O	AOUTR/SIO3	2/4/6/8/10/12/14/16 mA		Right channel of AUDIO Analog output
26	AOUTL	A/I/O	AOUTL/SIO2	2/4/6/8/10/12/14/16 mA		Left channel of AUDIO Analog output
27	ONOFF	AI				All-purpose hardware switch
28	BAT	PWRI				Battery Voltage input
29	VCC	PWRO				I/O power
30	VDD	PWRO				Digital core power
31	GPIO8	A/I/O	LRADC1	2/4/6/8/10/12/14/16 mA	Z	Bit8 of GPIO 1.LRADC1: Low resolution A/D input 1
32	GPIO3	A/I/O	TWI_SCL/UART_TX/PWM/TEMPADC	2/4/6/8/10/12/14/16 mA	Z	Bit3 of GPIO 1.TWI_SCL 2.UART_TX 3.PWM 4.TEPMADC:Temperature A/D input
33	GPIO10	I/O	UART_RX/SIRQ1/PWM	2/4/6/8/10/12/14/16 mA	Z	Bit10 of GPIO 1.UART_RX 2.SIRQ1 3.PWM
34	GPIO9	I/O	UART_TX/SIRQ0/PWM	2/4/6/8/10/12/14/16 mA	Z	Bit9 of GPIO 1.UART_TX 2.SIRQ0 3.PWM
35	SPI_CLK	O				Clock of SPI
36	SPI_MOSI	I/O	SPI_MOSI/SPI_MISO	2/4/6/8/10/12/14/16 mA		1. Master Output Slave Input of SPI 2. Master Input Slave Output of SPI
37	SPI_SS	O	SPI_SS/SPI_MOSI	2/4/6/8/10/12/14/16 mA		1. Chip Enable of SPI 2. Master Output Slave Input of SPI
38	GPIO0	I/O	SD_CMD	2/4/6/8/10/12/14/16 mA	Z	Bit0 of GPIO 1.Command of SD Card
39	GPIO1	I/O	SD_CLK/UART_RX	2/4/6/8/10/12/14/16 mA	Z	Bit1 of GPIO 1.Clock of SD Card 2.UART_RX
40	GPIO2	I/O	SD_DAT/UART_TX	2/4/6/8/10/12/14/16 mA	Z	Bit2 of GPIO 1.Data of SD Card 2.UART_TX
41	EPAD	GND				Exposed pad as ground

Note: H: high level; L:low level; Z: high resistance

1.6 Package and Drawings



QFN40L

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	--	--
h	0.30	0.35	0.40
L/F (mil)	150*150		

Figure 1-3 ATS2815 Package and Dimension

2 Bluetooth

- Bluetooth 4.2 dual mode support: simultaneous LE and BR/EDR
- Compatible with Bluetooth V4.1/4.0/2.1+EDR
- Support all packet types in basic rate and enhanced data rate
- Support SCO/eSCO link
- Support secure simple pairing
- Support low power mode (sniff/sniff sub-rating)
- Support multiple low energy states
- Support bitpool up to 53 in SBC decoding
- Bluetooth Piconet and Scatternet support

Performance

- Maximum Bluetooth transmitting power: >4dBm
- Bluetooth receiving sensitivity: <-88dBm

3 Processor Core

- 156MHz processor Core
- Internal RAM for data and program storage
- 4-channel DMA, including DMA0, DMA1, DMA2 and DMA3, support for transmission in burst 8 mode

4 Memory Controller

- Operation clock rate up to 156MHz
- Memory Management Unit (MMU)
- Providing channel for DMA accessing internal memory
- Providing channel for CPU accessing internal memory
- Arbitrate the priority of CPU and DMA accessing internal memory
- Providing address remap function, biggest mapping address space is 4G Byte

5 DMA Controller

5.1 Features

- DMA transmission is independent of the CPU.
- Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory.
- 4-channel DMA, including DMA0, DMA1, DMA2, and DMA3, supports for transmission in burst 8 mode. Only one of the four DMA channels can transfer data at the same time.
- DMA0/DMA1/DMA2/DMA3 transmission can be triggered on the occurrence of selected events as following
  - SD/MMC DRQ
  - UART-RX DRQ
  - UART-TX DRQ
- Each channel can send two interrupts to the CPU on completion of certain operational events as following:
  - DMA3HFIP
  - DMA2HFIP
  - DMA1HFIP
  - DMA0HFIP
  - DMA3TCIP
  - DMA2TCIP
  - DMA1TCIP
  - DMA0TCIP

5.2 Memory and Peripheral Access Description

5.2.1 DMA channel priority

The DMA can access the memory block, once the DMA obtains a highest priority and the DMA channel occupies the DMA bus according to the following internal priority table of DMA channels. The possible combinations of priority of each DMA channel are listed below:

Table 5-1 Priority of Each DMA Channel

Priority	Priority0 x0 (High Priority)	Priority1 x1	Priority2 x2	Priority3 x3 (Low Priority)
0	DMA0	DMA1	DMA2	DMA3
1	DMA1	DMA0	DMA2	DMA3
2	DMA2	DMA0	DMA1	DMA3
3	DMA3	DMA0	DMA1	DMA2

5.3 DMA Register List

Table 5-2 DMA Control Group Base Address

Name	Physical Base Address	KSEG1 Base Address
DMAController	0xC00C0000	0xC00C0000

Table 5-3 DMA Controller Register List

Offset	Register Name	Description

0x00000000	DMAPRIORITY	DMA priority register
0x00000004	DMAIP	DMA interrupt pending register
0x00000008	DMAIE	DMA interrupt enable register
0x00000010	DMA0CTL	DMA0 control register
0x00000014	DMA0SADDR	DMA0 source address register
0x00000018	DMA0DADDR	DMA0 destination address register
0x0000001c	DMA0FRAMELEN	DMA0 frame length register
0x00000020	DMA1CTL	DMA1 control register
0x00000024	DMA1SADDR	DMA1 source address register
0x00000028	DMA1DADDR	DMA1 destination address register
0x0000002c	DMA1FRAMELEN	DMA1 frame length register
0x00000030	DMA2CTL	DMA2 control register
0x00000034	DMA2SADDR	DMA2 source address register
0x00000038	DMA2DADDR	DMA2 destination address register
0x0000003c	DMA2FRAMELEN	DMA2 frame length register
0x00000040	DMA3CTL	DMA3 control register
0x00000044	DMA3SADDR	DMA3 source address register
0x00000048	DMA3DADDR	DMA3 destination address register
0x0000004c	DMA3FRAMELEN	DMA3 frame length register

5.4 DMA Register Description

5.4.1 DMAPRIORITY

DMAPRIORITY (DMA Priority Register, offset = 0x00000000)

Bit(s)	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1:0	PRIORITYTAB	DMA Priority table : 2'd0 : DMA0>DMA1>DMA2>DMA3 2'd1 : DMA1>DMA0>DMA2>DMA3 2'd2 : DMA2>DMA0>DMA1>DMA3 2'd3 : DMA3>DMA0>DMA1>DMA2	RW	0x0

5.4.2 DMAIP

DMAIP (DMA Interrupt Pending Register, offset = 0x00000004)

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11	DMA3HFIP	DMA3 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
10	DMA2HFIP	DMA2 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
9	DMA1HFIP	DMA1 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
8	DMA0HFIP	DMA0 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
7:4	-	Reserved	-	-
3	DMA3TCIP	DMA3 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
2	DMA2TCIP	DMA2 Transmission Complete IRQ Pending	RW	0x0

		This bit can be written '1' to clear.		
1	DMA1TCIP	DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
0	DMA0TCIP	DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0

5.4.3 DMAIE

DMAIE (DMA Interrupt Enable Register, offset = 0x00000008)

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11	DMA3HFIE	DMA3 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
10	DMA2HFIE	DMA2 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
9	DMA1HFIE	DMA1 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
8	DMA0HFIE	DMA0 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
7:4	-	Reserved	-	-
3	DMA3TCIE	DMA3 Transmission Complete IRQ Enable: 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	RW	0x0
2	DMA2TCIE	DMA2 Transmission Complete IRQ Enable: 0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt	RW	0x0
1	DMA1TCIE	DMA1 Transmission Complete IRQ Enable: 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt	RW	0x0
0	DMA0TCIE	DMA0 Transmission Complete IRQ Enable: 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt	RW	0x0

5.4.4 DMA0CTL

DMA0CTL (DMA0 control Register, offset = 0x00000010)

Bit(s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10:8	DSTTYPE	Destination type: 3'b000: memory 3'b011: UART0 TX FIFO Others: reserved	RW	0x0
7	-	Reserved	-	-
6:4	SRCTYPE	Source type: 3'b000: memory 3'b011: UART0 RX FIFO Others: reserved	RW	0x0
3:2	-	Reserved	-	-
1	RELOAD	Reload the DMA controller registers and start DMA	RW	0x0

		transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode		
0	DMA0START	DMA0 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.	RW	0x0

5.4.5 DMA0SADDR

DMA0SADDR (DMA0 Source Address Register, offset = 0x00000014)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:0	DMA0SADDR	The source address of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	RW	0x0

5.4.6 DMA0DADDR

DMA0DADDR (DMA0 Destination Address Register, offset = 0x00000018)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:0	DMA0DADDR	The destination address of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	RW	0x0

5.4.7 DMA0FRAMELEN

DMA0FRAMELEN (DMA0 Frame Length Register, offset = 0x0000001c)

Bit(s)	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0FRAMELEN	The frame length of DMA0 transmission.	RW	0x0

5.4.8 DMA1CTL

DMA1CTL (DMA1 control Register, offset = 0x00000020)

Bit(s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10:8	DSTTYPE	Destination type: 3'b000: memory 3'b011: UART0 TX FIFO Others: reserved	RW	0x0
7	-	Reserved	-	-
6:4	SRCTYPE	Source type: 3'b000: memory 3'b011: UART0 RX FIFO Others: reserved	RW	0x0
3:2	-	Reserved	-	-

1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA1START	DMA1 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA1 controller if the DMA1 transmission is complete or DMA1 transmission error occurs. This bit can be written '0' to abort DMA1 transmission.	RW	0x0

5.4.9 DMA1SADDR

DMA1SADDR (DMA1 Source Address Register, offset = 0x00000024)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:0	DMA1SADDR	The source address of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	RW	0x0

5.4.10 DMA1DADDR

DMA1DADDR (DMA1 Destination Address Register, offset = 0x00000028)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:0	DMA1DADDR	The destination address of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	RW	0x0

5.4.11 DMA1FRAMELEN

DMA1FRAMELEN (DMA1 Frame Length Register, offset = 0x0000002c)

Bit(s)	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1FRAMELEN	The frame length of DMA1 transmission.	RW	0x0

5.4.12 DMA2CTL

DMA2CTL (DMA2 control Register, offset = 0x00000030)

Bit(s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10:8	DSTTYPE	Destination type: 3'b000: memory 3'b011: UART0 TX FIFO Others: reserved	RW	0x0
7	-	Reserved	-	-
6:4	SRCTYPE	Source type: 3'b000: memory 3'b011: UART0 RX FIFO Others: reserved	RW	0x0

3:2	-	Reserved	-	-
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA2START	DMA2 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA2 controller if the DMA2 transmission is complete or DMA2 transmission error occurs. This bit can be written '0' to abort DMA2 transmission.	RW	0x0

5.4.13 DMA2SADDR

DMA2SADDR (DMA2 Source Address Register, offset = 0x00000034)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:0	DMA2SADDR	The source address of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	RW	0x0

5.4.14 DMA2DADDR

DMA2DADDR (DMA2 Destination Address Register, offset = 0x00000038)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:0	DMA2DADDR	The destination address of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	RW	0x0

5.4.15 DMA2FRAMELEN

DMA2FRAMELEN (DMA2 Frame Length Register, offset = 0x0000003c)

Bit(s)	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2FRAMELEN	The frame length of DMA2 transmission.	RW	0x0

5.4.16 DMA3CTL

DMA3CTL (DMA3 control Register, offset = 0x00000040)

Bit(s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10:8	DSTTYPE	Destination type: 3'b000: memory 3'b011: UART0 TX FIFO Others: reserved	RW	0x0
7	-	Reserved	-	-
6:4	SRCTYPE	Source type: 3'b000: memory 3'b011: UART0 RX FIFO	RW	0x0

		Others: reserved		
3:2	-	Reserved	-	-
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA3START	DMA3 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA3 controller if the DMA3 transmission is complete or DMA3 transmission error occurs. This bit can be written '0' to abort DMA3 transmission.	RW	0x0

5.4.17 DMA3SADDR

DMA3SADDR (DMA3 Source Address Register, offset = 0x00000044)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:0	DMA3SADDR	The source address of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	RW	0x0

5.4.18 DMA3DADDR

DMA3DADDR (DMA3 Destination Address Register 0, offset = 0x00000048)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:0	DMA3DADDR	The destination address of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	RW	0x0

5.4.19 DMA3FRAMELEN

DMA3FRAMELEN (DMA3 Frame Length Register, offset = 0x0000004c)

Bit(s)	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3FRAMELEN	The frame length of DMA3 transmission.	RW	0x0

6 PMU

6.1 Features

The ATS2815 integrates a comprehensive power supply system, including the following features:

- Support Li-Ion battery power supply with battery insert wake up.
- Do not support USB power supply and USB insert wake up.
- Support power on button & reset button.
- Linear regulators output VCC, AVCC and VDD.
- Standby current 35uA (typical).
- Low precision A/D converters for Battery voltage monitor, temperature monitor and wire-controller.

6.2 Module Description

6.2.1 Linear Regulators

The ATS2815 integrates multiple linear regulators; they generate VCC, VDD and AVCC.

6.2.1.1 Regulators Accurate and Maximum Output Current

The output voltages are precisely within ±2%. Table below shows data of maximum output current.

Table 6-1 Regulators Maximum Output Current

LDOs	Input Voltage (V)	Default Output Voltage (V)	Load Capacity (mA)
VCC	BAT(3.4)	3.1	300
AVCC	VCC(3.1)	2.95	40
VDD	VCC(3.1)	1.2	50

6.2.1.2 Regulators Power Down

If the system is to operate from an external power supply, then the internal linear regulators are powered down automatically.

6.2.2 A/D Converters

There are 2 low resolutions 7 bit A/Ds for system monitor, one multiplexed for TEMPADC and BATADC multiplexing, another multiplexed for LRADC1 and LRADC2. And the input voltage range are 0.7V to 2.2V at TEMPADC pin, 1.4V to 4.4V at VBAT pin and 0V to AVCC at LRADC1 and LRADC2.

6.3 Register List

Table 6-2 PMU block base address

Name	Physical Base Address	KSEG1 Base Address
PMU	0xc0020000	0xc0020000

Table 6-3 PMU Block Configuration Registers List

Offset	Register Name	Description
0x14	PMUADC_CTL	PMU ADC frequency and enable Register
0x18	LRADC2_DATA	LRADC2 data Register
0x1c	TEMPADC_DATA	TEMPADC data Register
0x28	LRADC1_DATA	LRADC1 data Register
0x2c	BATADC_DATA	BATADC data Register
0x3c	LRADC1_RES_SET	LRADC1 pull up resistor set Register
0x4c	WKEN_CTL	Wake up source select Register
0x50	WAKE_PD	Wake up source pending Register
0x54	ONOFF_KEY	On/off Key control Register

6.4 Register Description

6.4.1 PMUADC_CTL

PMUADC Control Register 0xd3

Offset = 0x14

Bit(s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	BATADC_FS	BAT/TEMP ADCs Frequency Source Select: 0: 125HZ 1: 250HZ	RW	1
6	LRADC_FS	LRADC12 Frequency Source Select: 0: 125Hz 1: 250Hz	RW	1
5	LRADC2_EN	7bit LRADC2 A/D enable. 0: disable 1: enable	RW	0
4	LRADC1_EN	7bit LRADC1 A/D enable. 0: disable 1: enable	RW	1
3:2	-	Reserved	-	-
1	TEMPADC_EN	TEMP A/D enable 0: disable 1: enable	RW	1
0	BATADC_EN	Battery A/D enable 0: disable 1: enable	RW	1

6.4.2 LRADC2_DATA

LRADC2 DATA Register

Offset = 0x18

Bit(s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6:0	LRADC2	7bit LRADC2 result. LRADC2 input voltage range is from 0 to AVCC.	R	x

6.4.3 TEMPADC_DATA

TEMPADC DATA Register

Offset = 0x1C

Bit(s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6:0	TEMPADC	7bit Voltage ADC result, used to detect TEMPADC voltage. Input voltage range is:0.7-2.2V	R	xx

6.4.4 LRADC1_DATA

LRADC1 DATA Register

Offset = 0x28

Bit(s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6:0	LRADC1	7bit LRADC1 result. LRADC1 input voltage range is from 0 to AVCC.	R	x

6.4.5 BATADC_DATA

BATADC DATA Register

Offset = 0x2C

Bit(s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6:0	BATADC	7bit Voltage ADC result, used to detect Battery voltage. Input voltage range is (Li-ion): 1.4-4.4V.	R	xx

6.4.6 LRADC1_RES_SET

LRADC1 pull up resistor set register 0x00

Offset = 0x3c

Bit(s)	Name	Description	Access	Reset
31:6	-	Reserved	-	-
5	R_SEL	LRADC1 pull up resistor select:: 0: use internal resistor, 100kOhm, 5% 1: use external resistor	R/W	0
4:0	-	Reserved	-	-

6.4.7 WKEN_CTL

Wake up source enable register 0x44b

Offset = 0x4C

Bit(s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	BATWK_EN	Battery insertion wake up enable: 0: disable 1: enable	RW	1
9:4	-	Reserved	-	-
3	RESET_WKEN	Reset key wake up enable: 0: disable	RW	1

		1: enable		
2	SHORT_WKEN	Onoff key short press wake up enable: 0: disable 1: enable	RW	0
1	LONG_WKEN	Onoff key long press wake up enable: 0: disable 1: enable	RW	1
0	-	Reserved	-	-

Note: delay about 1ms after modifying this register.

6.4.8 WAKE_PD

Wake up source pending register 0x0

Offset = 0x50

Bit(s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	BATIN_PD	Battery insertion wake up pending bit: 0: no battery insertion wake up 1: battery insertion wake up	RW	0
7	RESET_PD	Reset key press pending: 0: no reset key pressed 1: reset key pressed Write 1 to clear to 0	RW	0
6	LONG_PLAY	Long press Play key pending bit: 0: no long press on play key 1: long press on play key Write 1 to clear to 0	RW	0
5	-	Reserved	-	-
2	ONOFF_PD	ONOFF wake up pending bit: 0: no ONOFF wake up 1: ONOFF wake up Write 1 to clear to 0	RW	0
1:0	-	Reserved	-	-

Note: delay about 1ms after modifying this register.

6.4.9 ONOFF_KEY

ONOFF key control & detect register 0x80d0

Offset = 0x54

Bit(s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	RESTART_SET	RESET key function setting: 0: reset vdd domain register, generate pending 1: restart, press reset and enter standby, key uplift will wake up and enter active	RW	0

9:7	ONOFF_PRESS_TIME	ONOFF key time setting:
		000: 50ms < t < 0.125s, short press;
		t >= 0.125s, long press;
		001: 50ms < t < 0.25s, short press;
		t >= 0.25s, long press;
		010: 50ms < t < 0.5s, short press;
		t >= 0.5s, long press;
			RW	001

		011: 50ms < t < 1s, short press;
		t >= 1s, long press;
		100: 50ms < t < 1.5s, short press;
		t >= 2s, long press;
		101: 50ms < t < 2s, short press;
		t >= 2s, long press;
		110: 50ms < t < 3s, short press;
		t >= 3s, long press;
		111: 50ms < t < 4s, short press;
		t >= 4s, long press;		

6	ONOFF_RST_EN	ONOFF long press reset function: 0: disable 1: enable	RW	1
5:4	ONOFF_RST_T_SEL	Long press ONOFF key send reset signal, time selection: 00: 6s 01: 8s 10: 10s 11: 12s	RW	01
3:2	-	Reserved	-	-
1	ONOFF_PRESS_1	RESET/RESTART key pressed or not: 0: RESET key not pressed down 1: RESET key pressed down	R	0
0	ONOFF_PRESS_0	ONOFF key pressed or not: 0: ONOFF key not pressed down 1: ONOFF key pressed down	R	0

Note: delay about 1ms after modifying this register.

7 Audio

- Built-in stereo 16-bit input sigma-delta DACs, SNR>92dB, SNR (A-Weighting)>95dB, THD+N < -81dB
- Built-in mono 16-bit input sigma-delta ADC, SNR>85dB, SNR(A-Weighting)>88dB, THD+N < -72dB
- DAC supports sample rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48kHz
- ADC supports sample rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48kHz
- Support non-direct drive output.

8 System Control

8.1 RMU

8.1.1 Features

The RMU Controller of ATS2815 has following features:

- The RMU (Reset Management Unit) can reset all the peripherals.
- The MCU can enter power-saving mode by setting the registers of RMU.

8.1.2 Register List

Table 8-1 RMU digital part base address

Name	Physical Base Address	KSEG1 Base Address
RMU_DIGITAL	0xC0000000	0xC0000000

Table 8-2 RMU digital part register list

Offset	Register Name	Description
0x00000000	MRCR	Module Reset Control Register

8.1.3 Register Description

8.1.3.1 MRCR

MRCR (Module Reset Control Register, offset = 0x00000000)

Bit(s)	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	FMCLK_RESET	FMCLK Reset: 0: reset 1: normal	RW	0
12	AUDIO_RESET	AUDIO Controller Reset: 0: reset 1: normal	RW	0
11	SDC_RESET	SDC Controller Reset 0: reset 1: normal	RW	0
10:9	-	Reserved	-	-
8	PWM_RESET	PWM Controller Reset 0: reset 1: normal	RW	0
7	TWI_RESET	TWI Controller Reset 0: reset 1: normal	RW	0
6:5	-	Reserved	-	-
4	UART_RESET	UART Controller Reset 0: reset 1: normal	RW	0

3:1	-	Reserved	-	-
0	DMA_RESET	DMA Reset 0: reset 1: normal The reset bit of DMA controller is active while it is driven by MCU clock.	RW	0

8.2 CMU Digital

8.2.1 Features

The CMU (Clock Management Unit) Controller selects HOSC, CORE_PLL, CK_24M, CK_32K as the clock of each peripheral.

8.2.2 Register List

Table 8-3 CMU Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_Control_Register	0xC0001000	0xC0001000

Table 8-4 CMU Controller Registers

Offset	Register Name	Description
0x0000	CMU_SYSCLK	SYSCLK Control Register
0x0004	CMU_DEVCLKEN	DEVCLKEN Control Register
0x0010	CMU_SDCLK	SDCLK Control Register
0x0014	CMU_FMCLK	FMCLK Control Register
0x0018	CMU_PWMCLK	PWMCLK Control Register
0x001C	CMU_SPICLK	SPICLK Control Register
0x0020	CMU_UARTCLK	UARTCLK Control Register

8.2.3 Register Description

8.2.3.1 CMU_SYSCLK

CMU_SYSCLK Control register
Offset = 0x00

Bits	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8	AHBCLKDIV	S_CLK divisor 0: /2 1: /4	RW	0x0
7:6	-	Reserved	-	-
5:4	CPUCLKDIV	CPU_CLK divisor: 00: /1 01: /2 10: /4 11: /8	RW	0x0
3:2	-	Reserved	-	-
1:0	CORE_CLKSEL	CORE_CLK select: 00: CK_32K	RW	0x0

		01: HOSC 10: CORE_PLL 11: CK_52M		

8.2.3.2 CMU_DEVCLKEN

CMU_DEVCLKEN Control register
Offset = 0x04

Bits	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19	BT_RFCLK_EN	BT RF digital clock enable bit : 0: disable 1: enable	RW	0
18	BT_MODEMCLK_EN	BT MODEM clock enable bit: 0: disable; 1: enable;	RW	0
17	BT_BBCLK_EN	BT BB clock enable bit: 0: disable; 1: enable;	RW	0
16	BT_BB3P2K_EN	BT BB 3.2K clock enable bit: 0: disable; 1: enable;	RW	0
15:11	-	Reserved	-	-
10	FMCLKEN	FM clock enable bit: 0: disable 1: enable	RW	0x0
9	PWMCLKEN	PWM clock enable bit: 0: disable 1: enable	RW	0x0
8	DACCLKEN	DAC controller clock enable bit: 0: disable 1: enable	RW	0x0
7	ADCCLKEN	ADC controller clock enable bit: 0: disable 1: enable	RW	0x0
6	SPICLKEN	SPI controller clock enable bit: 0: disable 1: enable	RW	0x0
5	TWICLKEN	TWI controller clock enable bit: 0: disable 1: enable	RW	0x0
4	UARTCLKEN	UART controller clock enable bit: 0: disable 1: enable	RW	0x0
3	-	Reserved	-	-
2	USBCLKEN	USB controller clock enable bit: 0: disable 1: enable	RW	0x0
1	SDCLKEN	SD card controller clock enable bit: 0: disable 1: enable	RW	0x0
0	DMACLKEN	DMA clock enable bit: 0: disable	RW	0x0

		1: enable		

8.2.3.3 CMU_SDCLK

CMU_SDCLK Control register
Offset = 0x10

Bits	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	SDCLKSEL1	SD card controller clock select 1: 0: /1 1: /256	RW	0x0
7:5	-	Reserved	-	-
4	SDCLKSEL0	SD card controller clock select 0: 0: HOSC 1: CORE_PLL	RW	0x0
3	-	Reserved	-	-
2:0	SDCLKDIV	SD_CLK divisor 000: /1 001: /2 010: /3 011: /4 100: /5 101: /6 110: /7 111: /8	RW	0x0

8.2.3.4 CMU_FMCLK

CMU_FMCLK Control register
Offset = 0x14

Bits	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1:0	FMCLKSEL	FM clock select: 00: CK_32K 01: HOSC 10: CORE_PLL/10 11: CK_24M	RW	0x0

8.2.3.5 CMU_PWMCLK

CMU_PWMCLK Control register
Offset = 0x18

Bits	Name	Description	Access	Reset
31:9	-	Reserved	-	-
12	PWMCLKSEL	PWM controller clock select: 0: CK_32K 1: HOSC	RW	0x0
11:9	-	Reserved	-	-
8:0	PWMCLKDIV	PWM controller clock divisor: 0: /1 1: /2 …	RW	0x0

		255: /256 256: /512 257: /1024 258~511: reserved		

8.2.3.6 CMU_SPICLK

CMU_SPICLK Control register
Offset = 0x1C

Bits	Name	Description	Access	Reset
31:6	-	Reserved	-	-
5:4	SEL	SPI_CLK clock select: 00: CPU_CLK 01: HOSC 10: CORE_PLL 11: CK_48M	RW	0x0
3:0	DIV	SPI controller clock divisor: 0: /1 1: /2 2: /4 3: /6 4: /8 … 15: /30	RW	0x0

8.2.3.7 CMU_UARTCLK

CMU_UARTCLK Control register
Offset = 0x20

Bits	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	SEL	UART clock select: 0: HOSC 1: CK_24M	RW	0x0

8.3 CMU Analog

8.3.1 Features

- Support only one oscillator input: 26MHz

8.3.2 Register List

Table 8-5 CMU Analog Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_Analog_Register	0xC0000100	0xC0000100

Table 8-6 CMU Analog Controller Registers

Offset	Register Name	Description

0x00	HOSC_CTL	HOSC control register

8.3.3 Register Description

8.3.3.1 HOSC_CTL

HOSC control register.
Offset = 0x00(VDD domain)

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18:17	coarse_cap_xi	HOSCI PAD base cap select: 00: 0p 01: 5p 10: 10p 11: 15p	RW	10
16:12	fine_cap_xi	HOSCI PAD trim cap select	RW	0x00
11	-	Reserved	-	-
10:9	coarse_cap_xo	HOSCO PAD base cap select: 00: 0p 01: 5p 10: 10p 11: 15p	RW	10
8:4	fine_cap_xo	HOSCO PAD trim cap select	RW	0x00
3:1	-	Reserved	-	-
0	HOSC_EN	HOSC enable: 0: disable 1: enable	RW	1

8.4 Watchdog Timer

8.4.1 Features

- Built-in 32kHz oscillator
- A watch dog which can be configured as IRQ or Reset

8.4.2 Register List

Table 8-7 TIMER block base address

Name	Physical Base Address	KSEG1 Base Address
TIMER	0xC0120000	0xC0120000

Table 8-8 TIMER Controller Registers

Offset	Register Name	Description
0x04	WD_CTL	Watch Dog Control register

8.4.3 Register Description

8.4.3.1 WD_CTL

Offset=0x04(VDD)

Bits	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6	IRQP	Watch dog IRQ pending bit, writing 1 to this bit will clear it	RW	0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select.0: Reset,1: IRQ-. 0: Send Reset signal when watchdog overflow. 1: Send IRQ signal when watchdog overflow.	RW	0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot.	RW	0
3:1	CLKSEL	Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length The watch dog's overflow value is 180. 000 1khz 176 ms 001 512hz 352 ms 010 256hz 703ms 011 128hz 1.4 s 100 64hz 2.8s 101 32hz 5.6 s 110 16hz 11.2s 111 11.25ms	RW	0
0	CLR	Clear bit, write 1 to clear WD timer, cleared automatically	RW	0

8.5 INTC (Exceptions and Interrupts Controller)

8.5.1 Features

The ATS2815 uses RISC32 processor. The ATS2815 also adds additional controller to manage up to 32 interrupt sources.

Table below shows all interrupt sources.

Table 8-9 Interrupt sources

Interrupt Number	Sources	Type
0	Reserved	-
1	PMU	High Level
2	WatchDog	High Level
3~5	Reserved	-
6	UART	High Level
7	SIRQ0	High Level
8	Reserved	-
9	SPI	High Level
10	Reserved	-
11	TWI	High Level
12	Reserved	-
13	SIRQ1	High Level

14	DAC	High Level
15	ADC	High Level
16	Reserved	-
17	Reserved	-
18	DMA0	High Level
19	DMA1	High Level
20	DMA2	High Level
21	DMA3	High Level
22~31	Reserved	-

8.5.2 Register List

The ATS2815 implements a controller to handle 32 interrupt request, the registers are listed below:

Table 8-10 Table Interrupt Controller base address

Name	Physical Base Address	KSEG1 Base Address
InterruptController	0xC00B0000	0xC00B0000

Table 8-11 Interrupt Controller Registers

Offset	Register Name	Description
0x00000000	INTC_PD	Interrupt Pending register
0x00000004	INTC_MSK	Interrupt Mask register
0x00000014	INTC_EXTCTL	External interrupt control register
0x00000018	INTC_EXTIP	External interrupt status register

8.5.3 Register Description

8.5.3.1 INTC_PD

INTC_PD (Interrupt Pending Register, offset = 0x00000000)

Bit(s)	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	DMA3_IP	DMA3 controller interrupt pending bit	R	0
20	DMA2_IP	DMA2 controller interrupt pending bit	R	0
19	DMA1_IP	DMA1 controller interrupt pending bit	R	0
18	DMA0_IP	DMA0 controller interrupt pending bit	R	0
17	-	Reserved	-	-
16	-	Reserved	-	-
15	ADC_IP	ADC interrupt pending bit	R	0
14	DAC_TX_IP	DAC interrupt pending bit	R	0
13	SIRQ1_IP	SIRQ1 interrupt pending bit	R	0
12	-	Reserved	-	-
11	TWI_IP	TWI interrupt pending bit	R	0
10	-	Reserved	-	-
9	SPI_IP	SPI interrupt pending bit	R	0
8	-	Reserved	-	-
7	SIRQ0_IP	SIRQ0 interrupt pending bit	R	0
6	UART_IP	UART interrupt pending bit	R	0
5:3	-	Reserved	-	-

2	WD_IP	WatchDog interrupt pending bit	R	0
1	PMU_IP	PMU pending	R	0
0	-	Reserved	-	-

Note:
(1) Interrupt Pending bits can not be cleared by writing 1. These bits are automatically cleared only by clear all the corresponding interrupt pending bits of the device register, otherwise unchanged.
(2) 0: no interrupt request; 1: interrupt request detected

8.5.3.2 INTC_MSK

INTC_MSK (Interrupt Mask Register, offset = 0x00000004)

Bit(s)	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	DMA3_IM	DMA3 controller interrupt mask bit	RW	0
20	DMA2_IM	DMA2 controller interrupt mask bit	RW	0
19	DMA1_IM	DMA1 controller interrupt mask bit	RW	0
18	DMA0_IM	DMA0 controller interrupt mask bit	RW	0
17	-	Reserved	-	-
16	-	Reserved	-	-
15	ADC_IM	ADC interrupt mask bit	RW	0
14	DAC_TX_IM	DAC interrupt mask bit	RW	0
13	SIRQ1_IM	SIRQ1 interrupt mask bit	RW	0
12	-	Reserved	-	-
11	TWI_IM	TWI interrupt mask bit	RW	0
10	-	Reserved	-	-
9	SPI_IM	SPI interrupt mask bit	RW	0
8	-	Reserved	-	-
7	SIRQ0_IM	SIRQ0 interrupt mask bit	RW	0
6	UART_IM	UART interrupt mask bit	RW	0
5:3	-	Reserved	-	-
2	WD_IM	WatchDog interrupt mask bit	RW	0
1	PMU_IM	PMU interrupt mask bit	RW	0
0	-	Reserved	-	-

Note:
0: Interrupt is masked. 1: Interrupt is unmasked.

8.5.3.3 INTC_EXTCTL

INTC_EXTCTL (External Interrupt Control register, offset = 0x00000014)

Bit(s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	EXTYPE1	External Interrupt 1 Type 0: Rising edge-triggered; 1: Falling edge-triggered.	RW	0
2	-	Reserved	-	-
1	EXTYPE0	External Interrupt 0 Type 0: Rising edge-triggered; 1: Falling edge-triggered.	RW	0
0	-	Reserved	-	-

8.5.3.4 INTC_EXTIP

INTC_IP (External Interrupt Pending register, offset = 0x00000018)

Bit(s)	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	E1PD	External Interrupt 1 Pending 0: External interrupt source 1 is not active. 1: External interrupt source 1 is active. Write 1 to will clear this bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0
0	E0PD	External Interrupt 0 Pending 0: External interrupt source 0 is not active. 1: External interrupt source 0 is active. Write 1 to will clear this bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0

9 Storage

SD/MMC Card Controller Features

- Fully compliant with MMC Specification 4.0
- Fully compliant with SD card Specification 2.0
- Integrated Watchdog timeout Counter to report Exception happening.
- Integrated Pull up resistance (value 51Komh) for Data and CMD Line.
- Integrated CRC calculate and check circuit.
- Support 3.1V CLK PAD voltage.
- Support 3.1V CMD PAD voltage.
- Support 3.1V DAT PAD voltage.
- Maximal SD interface Clock: 50MHz
- Support SD 1line bus.
- Band Width: 6.25MByte/S (max)

10 Transfer and Communication

10.1 USB

10.1.1 Features

- Comply with the USB1.1 Specification, support host or device mode
- Support point-to-point communication with one full-speed device in Host mode (no HUB support).
- Support full-speed in peripheral mode.
- Support 2 IN endpoint and 1 OUT endpoint except endpoint0.
- Support bulk Isochronous and Interrupt transfer.
- Partially configurable endpoint type and single, double triple or quad buffering.
- Integrated synchronous RAM as endpoint FIFOs.
- Support suspend, resume and power management function.
- Support remote wakeup.

10.1.2 Register List

Table 10-1 USB Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
USB_CONTROLLER_REGISTERS	0xC0080000	0xC0080000

Table 10-2 USB Controller Registers

Offset	Register Name	Description
0x419	LINESTATUS	Line status register
0x41A	DPDMCTRL	DPDM control register

10.1.3 Register Description

10.1.3.1 LINESTATUS

Line status register
Offset = 0x419

Bit (s)	Name	Description	Access	Reset
7:5	-	Reserved	-	-
4:3	USB_LS	USB linestate[1:0] Linestate0:DP Linestase1:DM	R	00
2:0	-	Reserved	-	-

10.1.3.2 DPDMCTRL

DP DM control register
Offset = 0x41A

Bit (s)	Name	Description	Access	Reset
7	-	Reserved	-	-

6	PLUGIN	This bit Indicated the USB connection status when Linedeten is enabled. 1: connect 0: disconnect	R	x
5	-	Reserved	-	-
4	LINEDETEN	Line status detect enable 1: enable 0: disable	RW	1
3	DMPUEN	500Kohm DM pull up resistor enable. 1: enable 0: disable	RW	1
2	DPPUEN	500Kohm DP pull up resistor enable. 1: enable 0: disable	RW	1
1	DMPDDIS	DM pull down disable. 1: disable 0: enable	RW	1
0	DPPDDIS	DP pull down disable. 1: disable 0: enable	RW	1

10.2 TWI

10.2.1 Features

- Only support slave mode
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Multi-master, Hi-speed mode and 10bit address mode not support
- Internal Pull-Up Resistor (10k) optional

10.2.2 Function Description

Two wire interfaces (TWI) bus is used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is TWI.
TWI provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available TWI devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. TWI is easy to use to link multiple devices together since it has a built-in addressing scheme.

Note:

1. *The TWI module is in Slave mode by default.*
2. *Generate the IRQ while the bus status changes.*
   - *A byte transfer complete, include transmit and receive data or address*
   - *A stop bit detected*
3. *Release the bus by software after receiving data or address.*

10.2.3 Operation Manual

Slave mode:

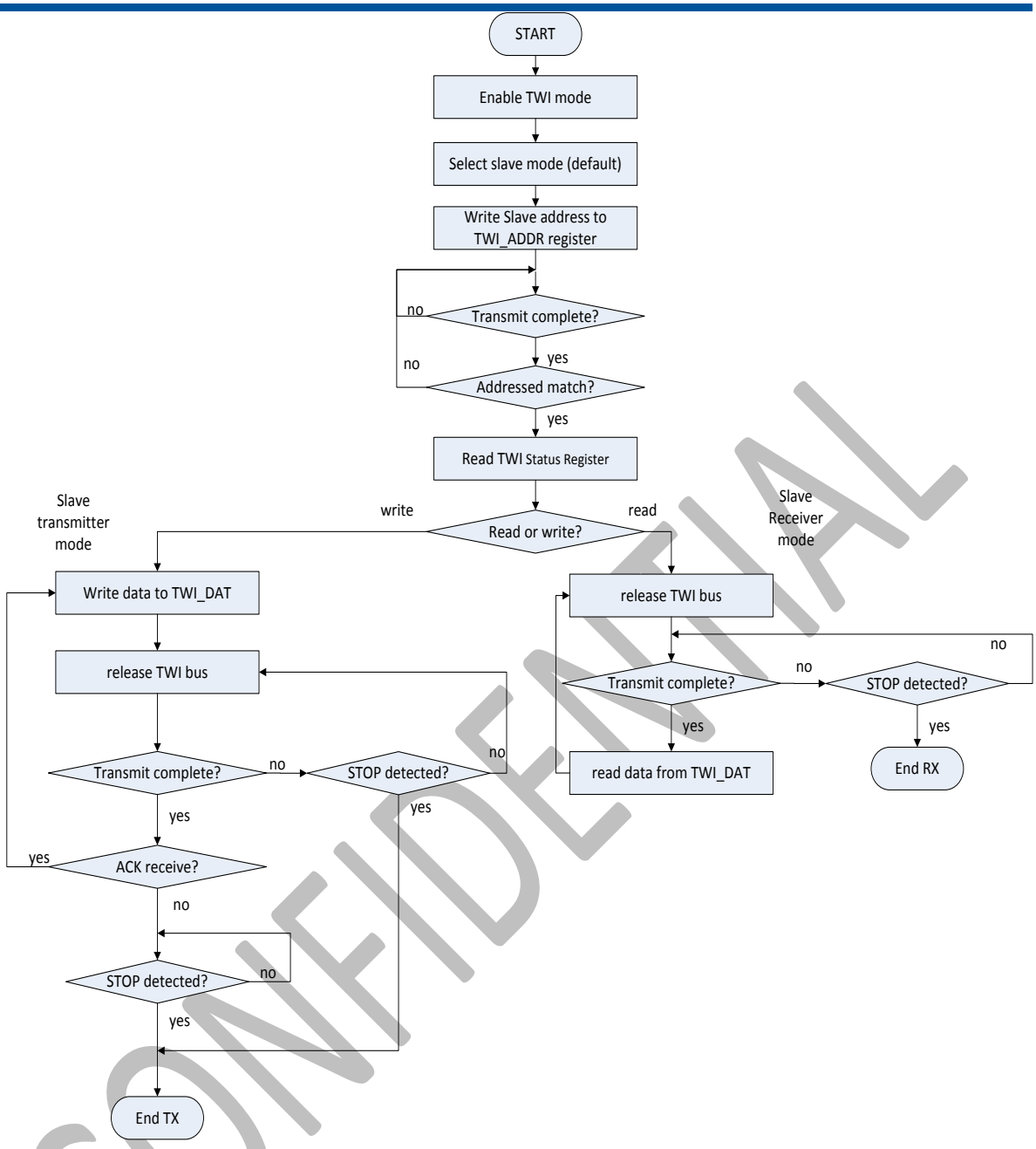


Figure 10-1 TWI Slave mode operation flow

10.2.4 Register List

Table 10-3 TWI Register Block Base Address

Name	Physical Base Address	KSEG1 Base Address
TWI	0xc0130000	0xc0130000

Table 10-4 TWI Registers Offset Address

Offset	Register Name	Description
0x0000	TWI_CTL	TWI Control Register
0x0004	TWI_STAT	TWI Status Register
0x0008	TWI_ADDR	TWI Address Register
0x000c	TWI_DAT	TWI Data Register

10.2.5 Register Description

10.2.5.1 TWI_CTL

TWI Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	EN	Enable. When disable, reset the status machine to IDLE. 0: Disable 1: Enable	RW	0
6:5	-	Reserved	-	-
4	IRQE	IRQ Enable. When the TWI status changes, generate IRQ.TWI can detect 3 status: complete a byte transfer, stop, bus error. 0: Disable 1: Enable	RW	0
3:2	-	Reserved	-	-
1	RB	Release Bus. Write 1 to this bit will release the bus. MCU should write 1 to this bit after transmitting or receiving the last bit of a whole transfer, or detecting STOP condition. This bit would be cleared by hardware.	RW	0
0	GACK	Generating Acknowledge signal. In receive mode: 0: Generating the ACK signal to the transmitter at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	RW	0

10.2.5.2 TWI_STAT

TWI Status Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31: 9	-	Reserved	-	-
8	TCB	Transfer Complete Bit 0: not finish transfer 1: A byte transfer finish, include transfer the ACK or NACK bit Write “1” to clear this bit	RW	0
7	STPD	Stop Detect bit Writing 1 to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected	RW	0
6	STAD	Start Detect bit, include restart. Writing 1 to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	RW	0

5	RWST	Read/Write Status bit for slave mode. When in slave mode, this bit reflects the master device read from or write to the slave device if the last address is matched. This bit is valid before the next start bit, stop bit or NAK bit occurred. 1: Read 0: Write	R	0
4	LBST	Last Byte Status bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data	R	0
3	IRQP	IRQ Pending bit. Writing 1 to this bit will clear it. 1: IRQ 0: No IRQ	RW	0
2	BBB	Bus Busy Bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0
1	BEB	Bus Error Bit 0: No error occur 1: Bus error occur Write “1” to clear this bit Generate error bit when following conditions occur: Detect stop bit right after detecting start/restart bit. Detect stop start bit when sending or receiving data.	RW	0
0	RACK	In transmit mode: 0: Has not received the ACK signal 1: Has received the ACK signal. This bit will be cleared when the 9th clock of the next SCL arrived automatically.	R	0

10.2.5.3 TWI_ADDR

TWI Address Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:1	SDAD	Slave Device Address. In master mode, these bits are TWI slave device address. In slave mode, these bits are used to compare with the address that the master device sends out.	RW	0
0	-	Reserved	-	-

10.2.5.4 TWI_DAT

TWI Data Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	TXRXDAT	TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the	RW	0

		TWI-bus.		

10.3 UART

10.3.1 Features

ATS2815 support one UART interface, the UART has the following features:

- Support master or slave mode
- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- Capable of speeds up to 6Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system

10.3.2 Operation Manual

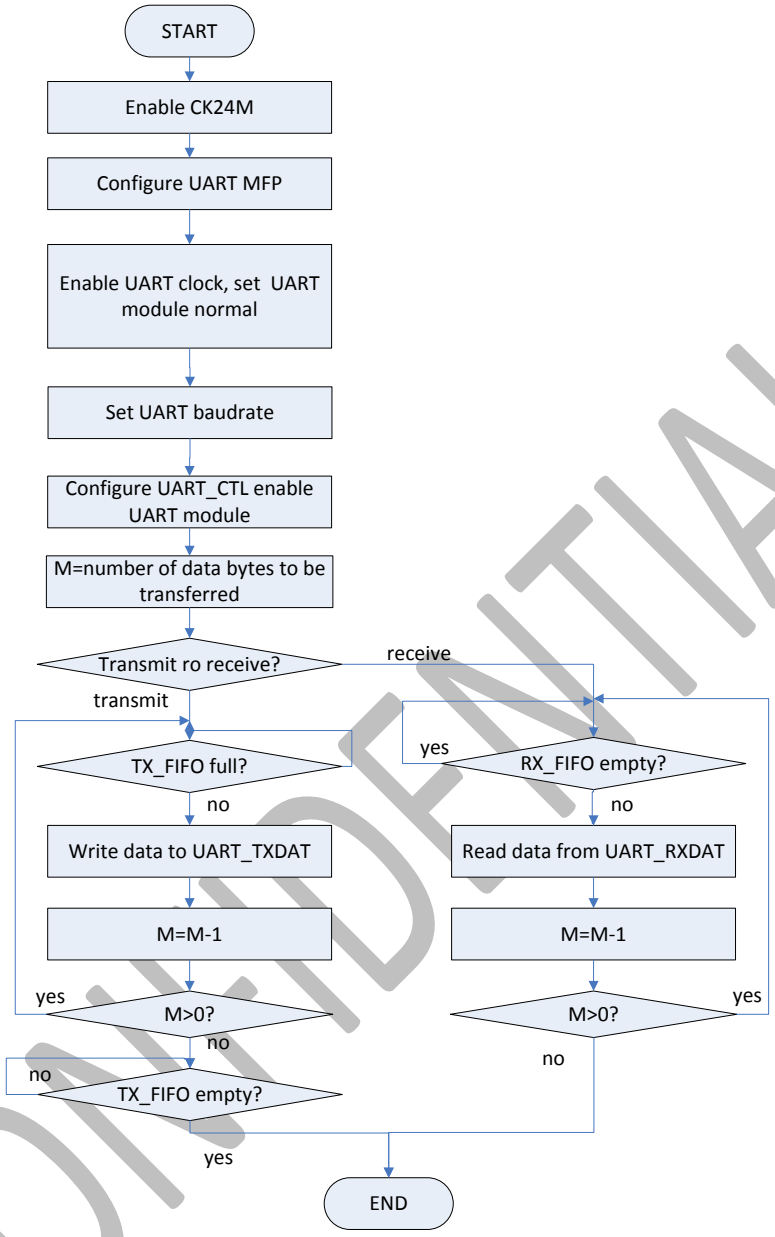


Figure 10-2 UART operation flow

10.3.3 Register List

Table 10-5 UART Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
UART	0xC01A0000	0xC01A0000

Table 10-6 UART Registers Offset Address

Offset	Register Name	Description
0x0000	UART_CTL	UART Control Register
0x0004	UART_RXDAT	UART Receive FIFO Data Register
0x0008	UART_TXDAT	UART Transmit FIFO Data Register
0x000C	UART_STA	UART Status Register

0x0010	UART_BR	BAUDRATE divider register

10.3.4 Register Description

10.3.4.1 UART_CTL

UART Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	RXDISABLE	UART RX disable 0: normal 1: disable	RW	0
30	TXDISABLE	UART TX disable 0: normal 1: disable	RW	0
29:24	-	Reserved	-	-
23	TX_FIFO_EN	UART TX FIFO enable: 0: Disable 1: Enable	RW	0
22	RX_FIFO_EN	UART RX FIFO enable: 0: Disable 1: Enable	RW	0
21	TXAHB_DMA_SEL	UART TX FIFO Clock Select 0: AHB Clock 1:DMA Clock	RW	0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the output will be presented on the input. And if we enable AFE, UART_RST's output will be presented on UART_CTS. 0: Disable 1: Enable	RW	0
19	TXIE	UART TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE	UART RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE	UART TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE	UART RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN	UART Enable. 0:disable 1: enable	RW	0
14	RXAHB_DMA_SEL	UART RX FIFO Clock Select 0: AHB Clock 1:DMA Clock	RW	0
13	RTSE	RTS Enable.	RW	0

		When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0: request to send data 1: no request		
12	AFE	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	RW	0
11:10	RDIC	UART RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00,01 because at least 8 bytes necessary.	RW	00
9:8	TDIC	UART TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00,01 because at least 8 bytes necessary.	RW	00
7	CTSE	CTS Enable. If this bit is 1, the transmitter checks CTS- before sending the next data byte. Note: This bit has no effect if Autoflow enable bit is set. 0: do not checks CTS- before sending 1: checks CTS- before sending	RW	0
6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	RW	000
3	-	Reserved	-	-
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. 0: 1 stop bit	RW	0

		1: 2 stop bit		
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	00

10.3.4.2 UART_RXDAT

UART Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×16levels.	R	X

10.3.4.3 UART_TXDAT

UART Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	TXDAT	Transmitted Data. The depth of FIFO is 8bit×16 levels	W	0

10.3.4.4 UART_STA

UART Status Register

Offset=0x000c

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23	PAER	Parity Status. 0: Parity OK 1: Parity error. Writing 1 to the bit will clear the bit. When parity error.	RW	0
22	STER	Stop Status. 0: Stop OK 1: Stop error. Writing 1 to the bit will clear the bit. When stop bit detect error.	RW	0
21	UTBB	UART TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0
20:16	TXFL	TX FIFO Level. The field indicates the current TX FIFO empty level.	R	10000
15:11	RXFL	RX FIFO Level. The field indicates the current RX FIFO level of valid data.	R	0
10	TFES	TX FIFO empty Status 0: no empty	R	1

		1: empty		
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8	RTSS	RTS Status. The bit reflects the status of the external RTS- pin.	R	0
7	CTSS	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit. When clock error.	RW	0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit.	RW	0
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit.	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	1
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

10.3.4.5 UART_BR

UART BAUDRATE divider register

Offset=0x0010

Bits	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	TXBRDIV	UART TX BAUDRATE divider BaudRate = Colck_source/BaudRate diveder Clock_source=HOSC or CK24M, selected by CMU_UARTCLK[0]	RW	0x028
15:12	-	Reserved	-	-
11:0	RXBRDIV	UART RX BAUDRATE divider BaudRate = Colck_source/BaudRate diveder Clock_source=HOSC or CK24M, selected by CMU_UARTCLK[0]	RW	0x0028

11 GPIO and I/O Multiplexer

11.1 Features

GPIO (General Purpose Input /Output) MFP:

GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers. But the PADs are limited, so MFP module is designed for multiplexing these PADs. Features of GPIO are listed below:

- Support 15 GPIOs
- All PADs have internal pull down resistors (100KOhm) or pull up resistors (100KOhm)
- Driving strength adjustable
- Automatically switching PAD function

PWM is multiplexing with GPIO, features of PWM are listed below:

- Support 1 PWM output
- Frequency ranges from 0.015625Hz~80K, adjustable. Under normal mode, PWM can output 256 kinds of duty cycles
- Breath mode PWM supports various frequency breathing lights.

SIO (Special Input /Output) MFP:

- 4 Special I/O ports bring more flexible application possibility.

Settings in actual practice please consult our engineers. The multiplexing relationship can be found in *Pin Description list.*

11.2 Operation Manual

11.2.1 Block Diagram

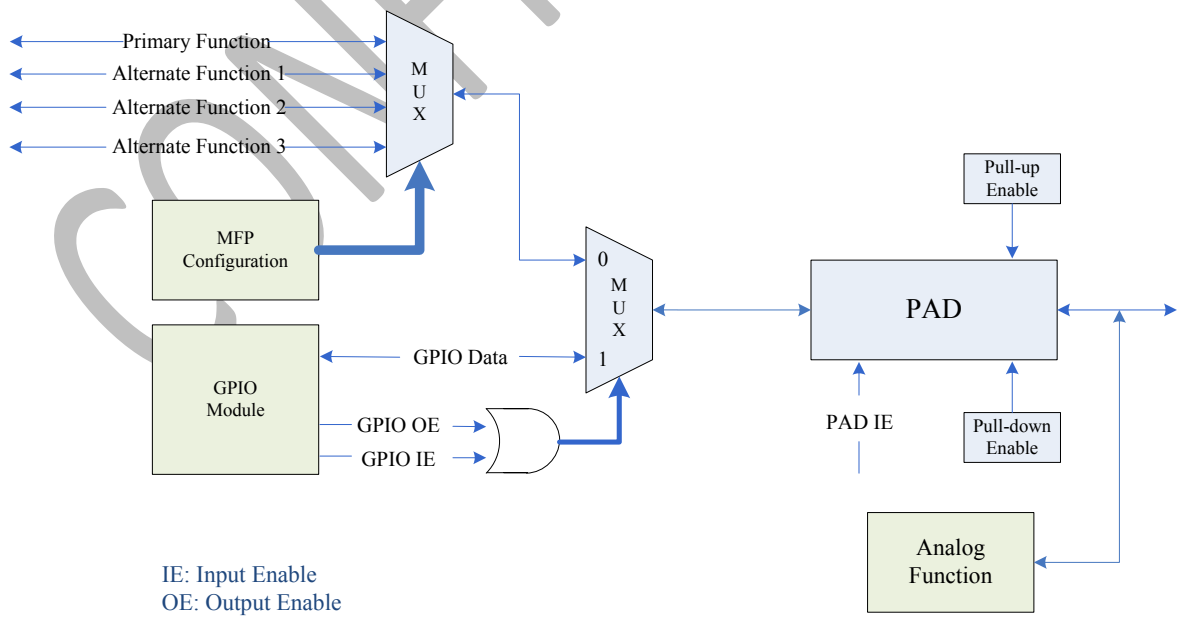


Figure 11-1 Block Diagram of GPIO controller

11.2.2 Multi-function Switch Operation

1. Some pin can be multiplexed as three kinds of functions: module function (MFP), GPIO function, Analog function, which can be configured by setting registers of MFP_CTL, GPIOINEN / GPIOOUTEN, and AD_SELECT.
2. The function priority of some multiplexed pin are Analog function > GPIO function > MFP function. GPIO and MFP are digital functions.
3. Some pin can be multiplexed as analog function and digital function. If the pin is used as digital function, analog function must be disabled firstly by setting AD_SELECT register.
4. Some MFP modules have their own pull-up and pull-down resistors, referring the chapter Pad PU control register and Pad PD control register; when the pin is multiplexed as MFP module function, the modules pull-up/pull-down resistors will be enabled automatically and the pull-up/pull-down resistors of GPIOs must be DISABLED, or the voltage level and functions will be abnormal.
5. The multiplexing register is AD_SELECT.

11.2.3 GPIO Output

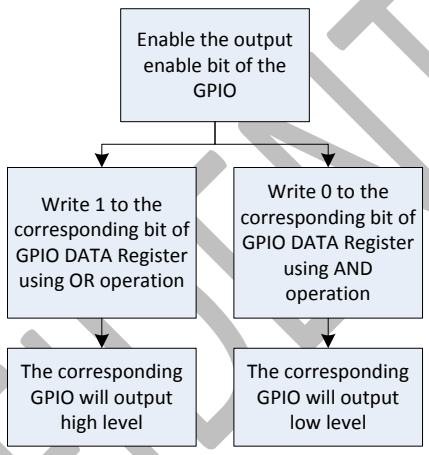


Figure 11-2 GPIO Output Configuration

11.2.4 GPIO Input

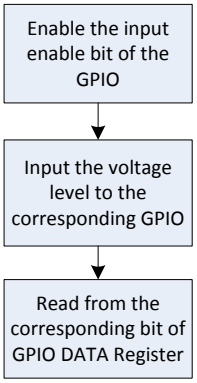


Figure 11-3 GPIO Input Configuration

11.2.5 SIO Output

Refer to the procedure as follows to configure an analog pin MICINL as a digital function such as SIO0.

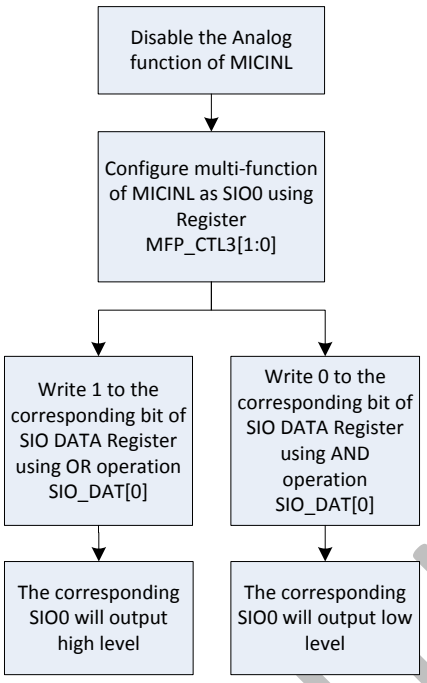


Figure 11-4 SDIO Output Configuration

11.2.6 GPIO Output/Input Loop Test

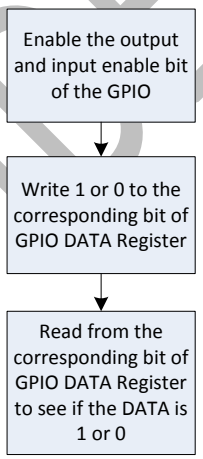


Figure 11-5 GPIO In/Out Loop Test

11.2.7 PWM Configure

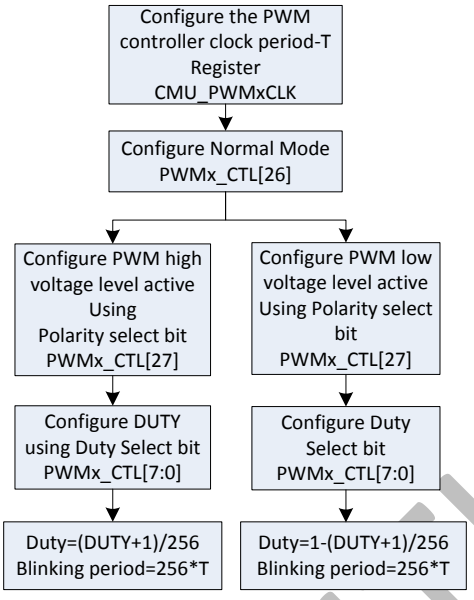


Figure 11-6 PWM Configuration

For example, if Duty =50% and the Blinking period is two seconds, T=2/256, the Frequency of the PWM controller clock is 1/T=128Hz, So CMU_PWMxCLK can be configured as 0xF9, PWMx_CTL can be configured as 0x0800007F.

11.3 Register List

Table 11-1 Table GPIO_MFP Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
GPIO_MFP	0xc0090000	0xc0090000

Table 11-2 GPIO&MFP Controller Registers

Offset	Register Name	Description	Voltage
GPIO Register			
0x0000	GPIOOUTEN	GPIO Output Enable	VDD
0x0004	GPIOINEN	GPIO Input Enable	VDD
0x0008	GPIODAT	GPIO Data	VDD
0x000C	GPIOPUEN	GPIO 100K PU Enable	VDD
0x0010	GPIOPDEN	GPIO 100K PD Enable	VDD
0x0014	SIO_OUTEN	SIO Output Enable	VDD
0x0018	SIO_INEN	SIO Input Enable	VDD
0x001C	SIO_DAT	SIO Data	VDD
0x0020	SIO_PUEN	SIO 100K PU Enable	VDD
0x0024	SIO_PDEN	SIO 100K PD Enable	VDD
PWM Register			
0x0028	PWM_CTL	PWM Output Control	VDD
MFP Register			
0x002C	MFP_CTL	Multiplexing Control	VDD
Analog/Digital Select Register			
0x0030	AD_Select	Analog/Digital Select	VDD
PAD Register			
0x0038	PADPUPD	PAD PU PD Resistance Enable	VDD
0x003C	PAD_SMIT	PAD Schmitt Control Register	VDD

0x0040	PADDRV0	PAD Drive Capacity Select 0	VDD
0x0044	PADDRV1	PAD Drive Capacity Select 1	VDD
0x0048	PADDRV2	PAD Drive Capacity Select 2	VDD

11.4 GPIO Register Description

11.4.1 GPIOOUTEN

GPIO Output Enable Register
Offset=0x00

Bit(s)	Name	Description	Access	Reset
31:15	-	Reserved	-	-
14:0	GPIOOUTEN	GPIO[14:0] Output Enable. 0: Disable 1: Enable	RW	0x0

11.4.2 GPIOINEN

GPIO Input Enable Register
Offset=0x04

Bit(s)	Name	Description	Access	Reset
31:15	-	Reserved	-	-
14:0	GPIOINEN	GPIO[14:0] Input Enable. 0: Disable 1: Enable	RW	0x0

11.4.3 GPIODAT

GPIO Data Register
Offset=0x08

Bit(s)	Name	Description	Access	Reset
31:15	-	Reserved	-	-
14:0	GPIODAT	GPIO[14:0] Input/Output Data.	RW	0x0

11.4.4 GPIOPUEN

GPIO 50K PU Enable Register
Offset=0x0C

Bit(s)	Name	Description	Access	Reset
31:15	-	Reserved	-	-
14:0	GPIOPUEN	GPIO[14:0] 100K PU Enable. 0: Disable 1: Enable	RW	0x0

11.4.5 GPIOPDEN

GPIOA 50K PD Enable Register
Offset=0x10

Bit(s)	Name	Description	Access	Reset
31:15	-	Reserved	-	-
14:0	GPIOPDEN	GPIO[14:0] 100K PD Enable. 0: Disable 1: Enable	RW	0x0

11.4.6 SIO_OUTEN

SpecialIO Output Enable Control Register
Offset = 0x14

Bit(s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	SIO_OUTEN	SpecialIO[3:0] Output Enable. 0: Disable 1: Enable	RW	0x0

11.4.7 SIO_INEN

SpecialIO Input Enable Control Register
Offset = 0x18

Bit(s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	SIO_INEN	SpecialIO[3:0] Input Enable. 0: Disable 1: Enable	RW	0x0

11.4.8 SIO_DAT

SpecialIO DATA Register
Offset = 0x1C

Bit(s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	SIO_DAT	SpecialIO[3:0] Input/Output Data.	RW	0x0

11.4.9 SIO_PUEN

SpecialIO PULL UP Enable Control Register
Offset = 0x20

Bit(s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	SIO_PUEN	SpecialIO[3:0] 100K PULL UP Enable. 0: Disable 1: Enable	RW	0x0

11.4.10 SIO_PDEN

SpecialIO PULL DOWN Enable Control Register
Offset = 0x24

Bit(s)	Name	Description	Access	Reset

31:4	-	Reserved	-	-
3:0	SIO_PDEN	SpecialIO[3:0] 100K PULL DOWN Enable. 0: Disable 1: Enable	RW	0x0

11.5 PWM Register Description

11.5.1 PWM_CTL

PWM Output Control Register
Offset=0x28

Bit(s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	Mode_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Time of increase and decline: T2=(Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

11.6 MFP Register Description

11.6.1 MFP_CTL

Multi-Function PAD Control Register
Offset=0x2C

Bit(s)	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	SPI_MISO_MFP	0:SPI_MISO MFP only usable on SPI PIN 1:SPI_MISO MFP only usable on GPIO7	RW	0x0
20	-	Reserved	-	-
19	GPIO14	0: Reserved 1: UART_RX	RW	0x0
18	GPIO13	0: Reserved 1: UART_TX	RW	0x0
17	GPIO12	0: DP 1: UART_RTS	RW	0x0

16	GPIO11	0: DM 1: UART_CTS	RW	0x0
15:14	GPIO10	00: Reserved 01: UART_RX 10: SIRQ1 11: PWM	RW	0x0
13:12	GPIO9	00: Reserved 01: UART_TX 10: SIRQ0 11: PWM	RW	0x0
11:10	GPIO7	00: Reserved 01: UART_RTS 10: PWM 11: SPI_MISO	RW	0x0
9:8	GPIO6	00: Reserved 01: UART_CTS 10: PWM 11: SIRQ1	RW	0x0
7:6	GPIO5	00: FMCLKOUT 01: UART_TX 10: SIRQ0 11: PWM	RW	0x0
5:4	GPIO4	00: TWI_SDA 01: UART_RX 10: PWM 11: Reserved	RW	0x0
3:2	GPIO3	00: TWI_SCL 01: UART_TX 10: PWM 11: Reserved	RW	0x0
1	GPIO2	0: SD_DAT0 1: UART_TX	RW	0x0
0	GPIO1	0: SD_CLK 1: UART_RX	RW	0x0

11.7 Analog/Digital Select Register Description

11.7.1 AD_Select

Analog/Digital Select Register
Offset=0x30

Bit(s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	GPIO6	0: GPIO6 is used as digital function, 1: Reserved	RW	0x0
6	AOUTR	0: AOUTR 1: SIO3	RW	0x0
5	AOUTL	0: AOUTL 1: SIO2	RW	0x0
4	AUXR	0: AUXR 1: SIO1	RW	0x0
3	AUXL	0: AUXL	RW	0x0

		1: SIO0		
2	GPIO3	0: GPIO3 is used as digital function, 1: GPIO3 is used as TEMPADC (Analog Function)	RW	0x0
1	GPIO4	0: GPIO4 is used as digital function, 1: GPIO4 is used as LRADC2 (Analog Function)	RW	0x0
0	GPIO8	0: GPIO8 is used as digital function, 1: GPIO8 is used as LRADC1 (Analog Function)	RW	0x0

11.8 PAD Register Description

11.8.1 PADPUPD

PAD PU PD Resistance Control Register
Offset=0x38

Bit(s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	TWI	TWI 10k PU Enable 0:Disable 1:Enable	RW	0x0
6	UART_RX	UART_RX 10k PU Enable 0:Disable 1:Enable	RW	0x0
5	SD_CMD	MMC/SD CMD 50k PU Enable 0:Disable 1:Enable	RW	0x0
4	SD_DAT	MMC/SD Data 50k PU Select 0:Disable 1:Enable	RW	0x0
3	SIRQ1PD	SIRQ1 100k PD Enable 0:Disable 1:Enable	RW	0x0
2	SIRQ1PU	SIRQ1 100k PU Enable 0:Disable 1:Enable	RW	0x0
1	SIRQ0PD	SIRQ0 100k PD Enable 0:Disable 1:Enable	RW	0x0
0	SIRQ0PU	SIRQ0 100k PU Enable 0:Disable 1:Enable	RW	0x0

11.8.2 PAD_SMIT

PAD Schmitt Control Register
Offset=0x3C

Bit(s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18	SPI_MISO	SPI_MISO PAD SMIT Enable 0:Disable 1:Enable	RW	0x0
17	SPI_MOSI	SPI_MOSI PAD SMIT Enable	RW	0x0

		0:Disable 1:Enable		
16	SPI_CLK	SPI_CLK PAD SMIT Enable 0:Disable 1:Enable	RW	0x0
15	SPI_SS	SPI_SS PAD SMIT Enable 0:Disable 1:Enable	RW	0x0
14:0	GPIO_SMIT_EN	GPIO[14:0] SMIT Enable 0:Disable 1:Enable	RW	0x0

11.8.3 PADDRV0

PAD Drive Control Register 0
Offset=0x40

Bit(s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:27	GPIO9	GPIO9 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1
26:24	GPIO8	GPIO8 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1
23:21	GPIO7	GPIO7 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1
20:18	GPIO6	GPIO6 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA	RW	0x1

		111:Level 8: 16mA		
17:15	GPIO5	GPIO5 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1
14:12	GPIO4	GPIO4 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1
11:9	GPIO3	GPIO3 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1
8:6	GPIO2	GPIO2 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1
5:3	GPIO1	GPIO1 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x3
2:0	GPIO0	GPIO0 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA	RW	0x1

		111:Level 8: 16mA		

11.8.4 PADDRV1

PAD Drive Control Register 1
Offset=0x44

Bit(s)	Name	Description	Access	Reset
31:27	-	Reserved	-	-
26:24	SPI_MISO	SPI_MISO PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x7
23:21	SPI_MOSI	SPI_MOSI PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x7
20:18	SPI_CLK	SPI_CLK PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x7
17:15	SPI_SS	SPI_SS PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x7
14:12	GPIO14	GPIO14 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1

11:9	GPIO13	GPIO13 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1
8:6	GPIO12	GPIO12 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x4
5:3	GPIO11	GPIO11 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x4
2:0	GPIO10	GPIO10 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x1

11.8.5 PADDRV2

PAD Drive Control Register 1
Offset=0x48

Bit(s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:9	SIO3	SIO3 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x0
8:6	SIO2	SIO2 PAD Drive Control	RW	0x0

		000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA		
5:3	SIO1	SIO1 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x0
2:0	SIO0	SIO0 PAD Drive Control 000:Level 1: 2mA 001:Level 2: 4mA 010:Level 3: 6mA 011:Level 4: 8mA 100:Level 5: 10mA 101:Level 6: 12mA 110:Level 7: 14mA 111:Level 8: 16mA	RW	0x0

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Table 12-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	TBD	TBD	°C
Storage temperature	Tstg	-55	+150	°C
ESD Stress voltage	Vesd (Human body model)	2000	-	V
Supply Voltage	BAT	3.0	5	V
	VCC/AVCC/VDDIF/VDDRF/VDDLO/VDDDAC	2.7	3.6	V
	VDD/VDDADC	0.8	1.5	V
Input Voltage	ONOFF	-	5	V
	3.3V IO	2.7	VCC+0.2	V

Note:
Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.

12.2 Recommended PWR Supply

Table 12-2 Recommended PWR Supply

Supply Voltage	Min	Typ	Max	Unit
BAT (Li)	3.3	3.8	4.3	V
VCC/ AVCC/VDDIF/VDDRF/VDDLO/VDDDAC	2.8	3.1	3.4	V
VDD	1.08	1.2	1.32	V
VDDADC	1.08	-	1.45	V

12.3 DC Characteristics

Table 12-3 DC Parameters for +3.3V IO Pin with Schmitt Trigger Off

Parameter	Symbol	Min.	Max.	Unit	Condition
Low-level input voltage	VIL	-	0.8	V	VCC = 3.1V Tamb = -10 to 70 °C
High-level input voltage	VIH	2.0	-	V	
Low-level output voltage	VOL	-	0.4	V	
High-level output voltage	VOH	2.4	-	V	

Table 12-4 DC Parameter for +3.3V IO Pin with Schmitt Trigger On

Parameter	Symbol	Min.	Max.	Unit	Condition
Schmitt trigger positive-going threshold	VT+	-	1.9	V	VCC=3.1V Tamb = -10 to 70 °C
Schmitt trigger negative-going threshold	VT-	1.2	-	V	

12.4 PWR Consumption

Table 12-5 PWR Consumption Table

VDD = 1.2V @ 25°C unless otherwise specified

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Standby	Is	Vbat = 3.8V;	-	35	60	uA

12.5 Bluetooth Characteristics

12.5.1 Transmitter

Table 12-6 Transmitter characteristics

VDD = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR	-	-	4	-	dBm
RF PWR Control Range	-	-	16	-	dB

12.5.2 Receiver

Table 12-7 Receiver Performance

Core Supply Voltage = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity	0.1% BER	-	-88	-	dBm

12.6 Mono Audio ADC

Table 12-8 Audio ADC Parameters

Pre-Amplifier						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Full Scale Input Voltage	THD+N < 1%		-	-	2.8	Vpp
Analogue gain	AUX OP	-	-12	-	7.5	dB
	MIC OP	Single Ended	-6	-	39	dB
Analogue to Digital Converter						
Resolution	-		-	-	16	Bits
Input Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz@Full Scale Input Voltage B/W = 22Hz~22kHz Fs=48kHz		-	85	-	dB
Dynamic Range	fin = 1kHz@-40dBFS Input Voltage B/W = 22Hz~22kHz Fs=48kHz		-	85	-	dB
THD+N	fin = 1kHz(input=1.6Vpp) B/W = 22Hz~22kHz Fs=48kHz		-	-72	-	dB
Digital gain	-		0	-	12	dB

12.7 Stereo DAC

Table 12-9 Stereo DAC Parameters

Digital to Analogue Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Output Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	92	-	dB
		A-Weighting	-	95	-	dB
Dynamic Range	fin = 1kHz@-48dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	88	-	dB
		A-Weighting	-	91	-	dB
THD+N	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	-81	-	dB
Digital gain	-		<-60	-	30.1	dB
Stereo crosstalk	fin = 1kHz@0dBFS input	-	-	-85	-	dB
PWR Amplifier						
Max Amplitude/PWR	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Single Ended Output	-	-	530	mVrms
			-	-	17	mW

Acronyms and Abbreviations

Abbreviations	Descriptions
AEC	Acoustic Echo Cancellers
ADC	Analog-to-Digital-Converter
CP0	Control Coprocessor 0
DAC	Digital-to-Analog-Converter
dBFS	dB Full Scale
DMA	Direct Memory Access
GPIO	General Purpose Input Output
HOSC	High Frequency OSC
INTC	Interrupt Controller
IRQ	Interrupt Request
MIC	Microphone
MMU	Memory Management Unit
MFP	Multiple Function PAD
OSC	Oscillator

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